
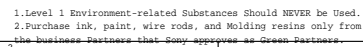


Page	Title of schematic page	Rev.	Date
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02	Block Diagram	1A	
03	Change List	1A	
04	ICS9LR3197	1A	
05	PROCESSOR 1/4(DMI&HOST&PCI)	1A	
06	PROCESSOR 2/4(DDR)	1A	
07	PROCESSOR 3/4(POWER)	1A	
08	PROCESSOR 4/4(GND)	1A	
09	PCH 1/5 (DMI&VIDEO)	1A	
10	PCH 2/5 (SATA/LPC/Azalia)	1A	
11	PCH 3/5 (PCI/PCIE/CLK/USB)	1A	
12	PCH 4/5 (GPIO)	1A	
13	PCH 5/5 (POWER)	1A	
14	DDR3 DIMM	1A	
15	CRT/LVDS	1A	
16	WWAN/Light Sensor	1A	
17	WPCE775L & FLASH	1A	
18	Docking/35001/TP/S1	1A	
19	HDD/ODD/SSD	1A	
20	KB/USB/FAN/Reset	1A	
21	HDMI	1A	
22	POWER CPU CORE (ISL62882)	1A	
23	POWER 3VPCU&5VPCU(PM6686)	1A	
24	POWER 1.5VSUS/VTT_MEM	1A	
25	POWER VCC1.05(OZ8111LN)-26A	1A	
26	POWER VCC_CFXCORE(MAX17028)	1A	
27	POWER(ADAPTER IN / CONN)	1A	
28	POWER VCC1.8	1A	
29	NVIDIA N11M-GE1 PCIE&PW 1/3	1A	
30	NVIDIA N11M-GE1 TMDS&DAC 2/3	1A	
31	NVIDIA N11M-GE1 VRAM 3/4	1A	
32	NVIDIA N11M-GE1 VRAM 4/4	1A	
33	R5U231	1A	

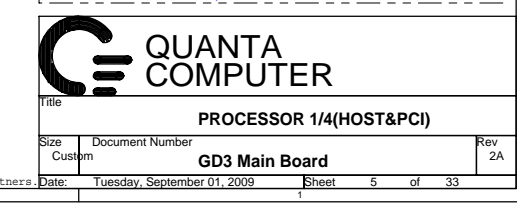
 QUANTA COMPUTER			
Title			
Page List			
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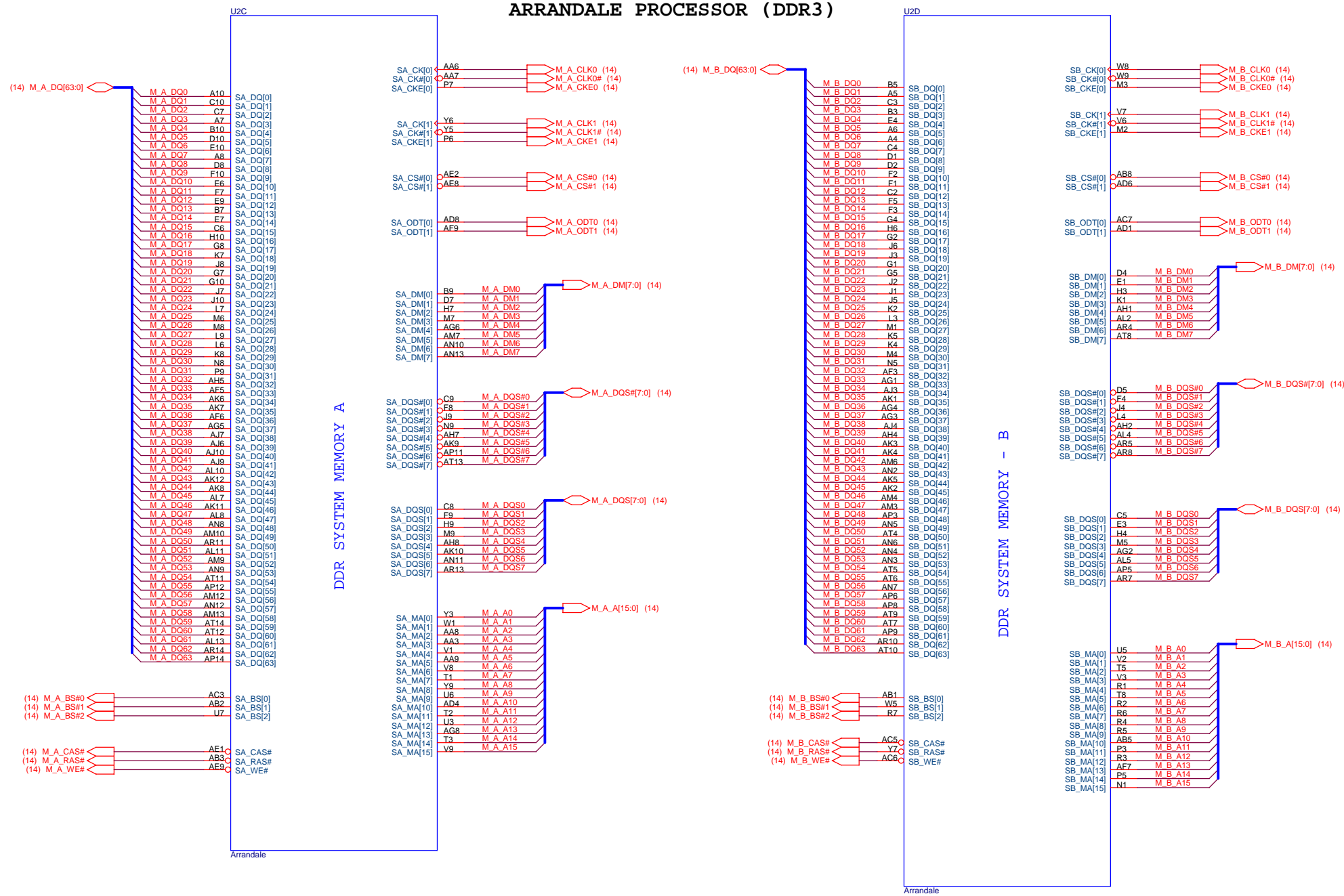
804

804

805



ARRANDALE PROCESSOR (DDR3)



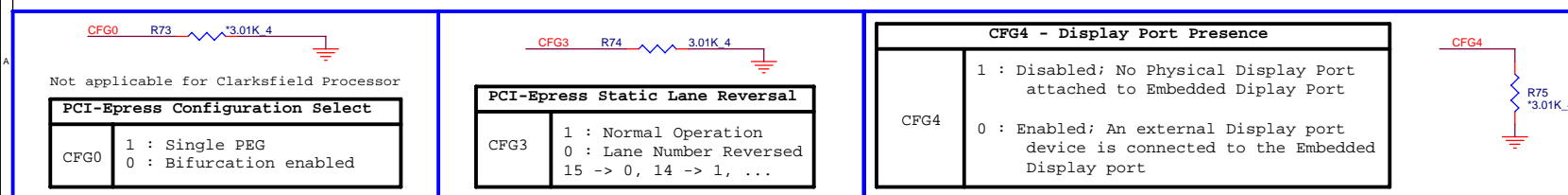
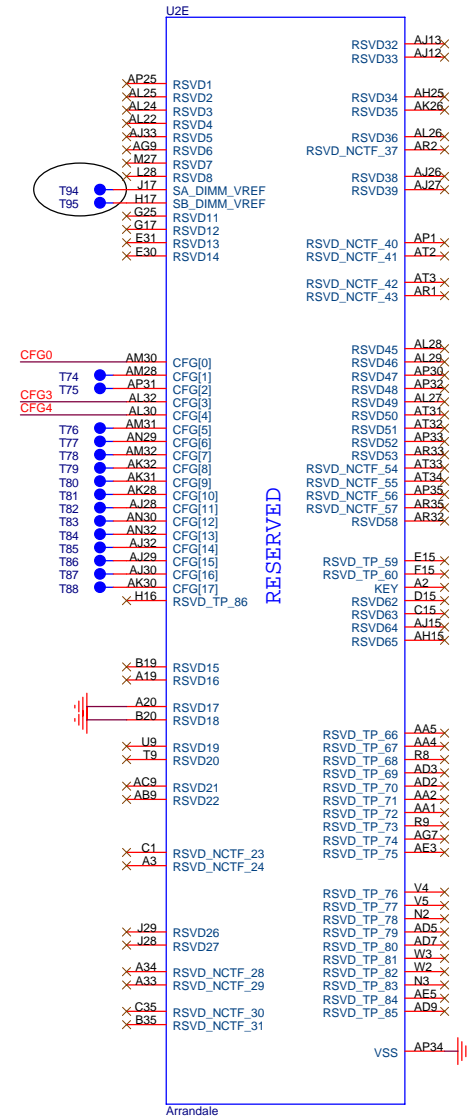
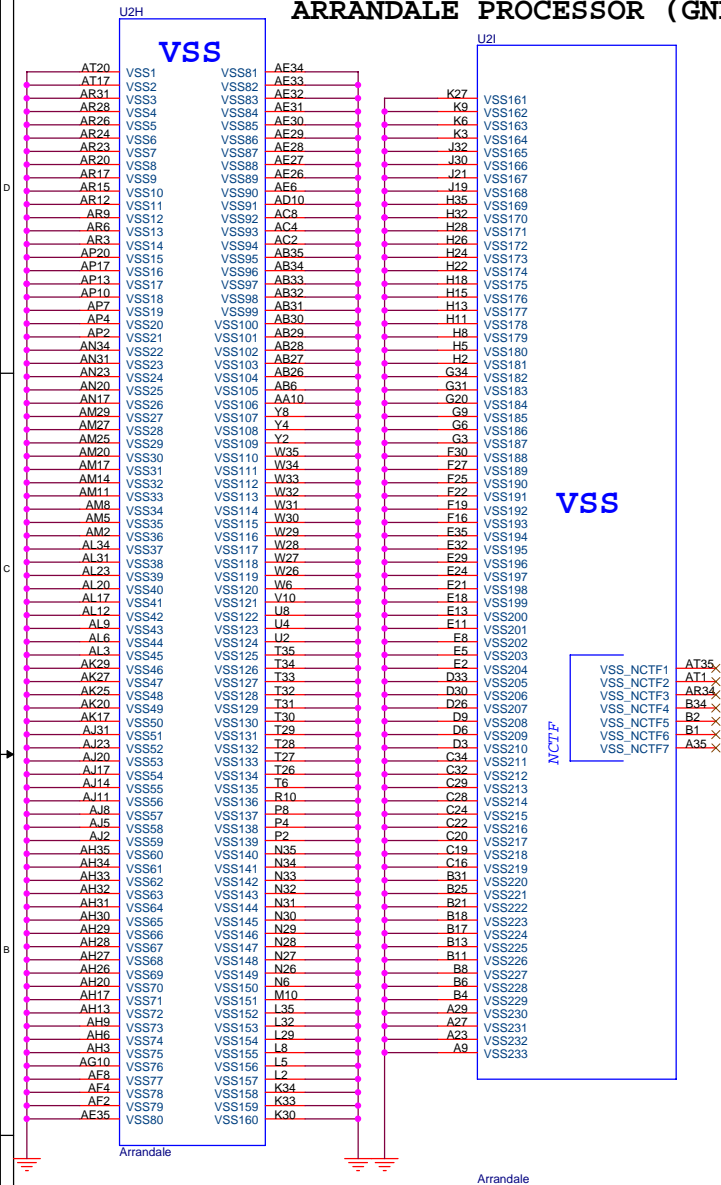


PROCESSOR 3/4(POWER)

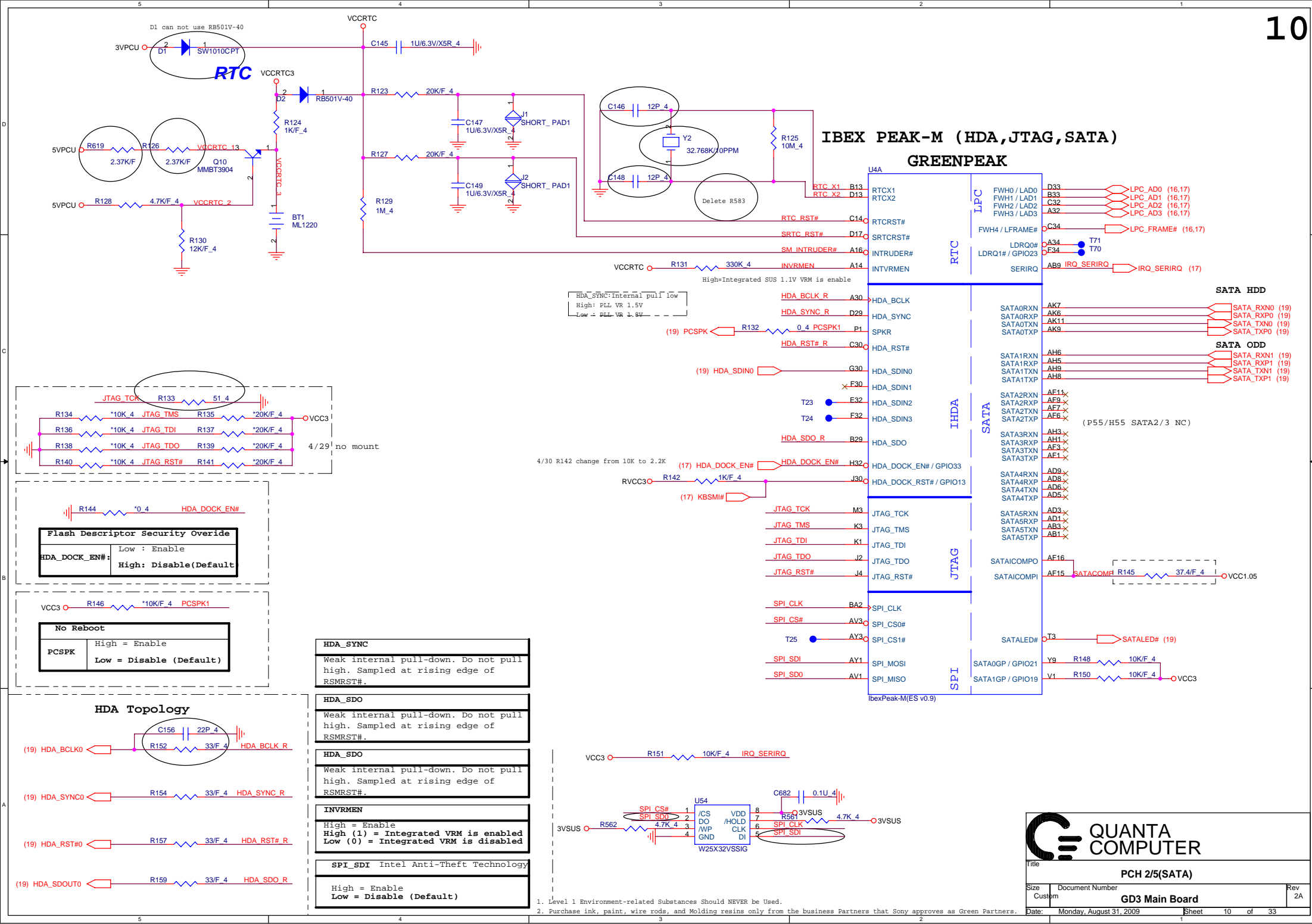
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Date: Monday, August 31, 2009	Sheet 7 of 33	

1. Level 1 Environment-related Substances Should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners

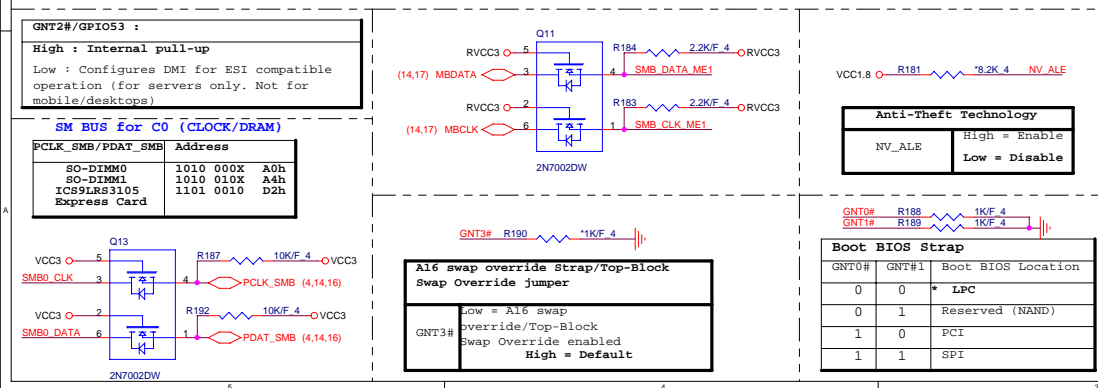
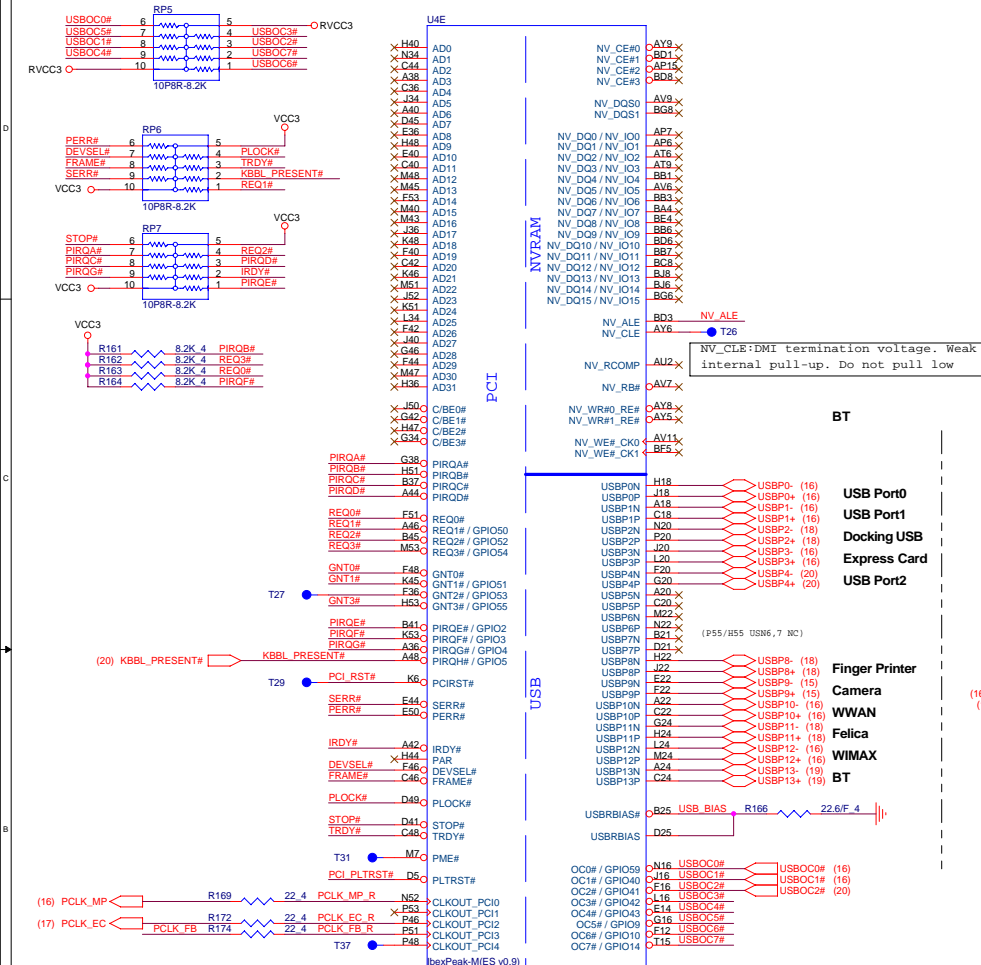
ARRANDALE PROCESSOR (GND)



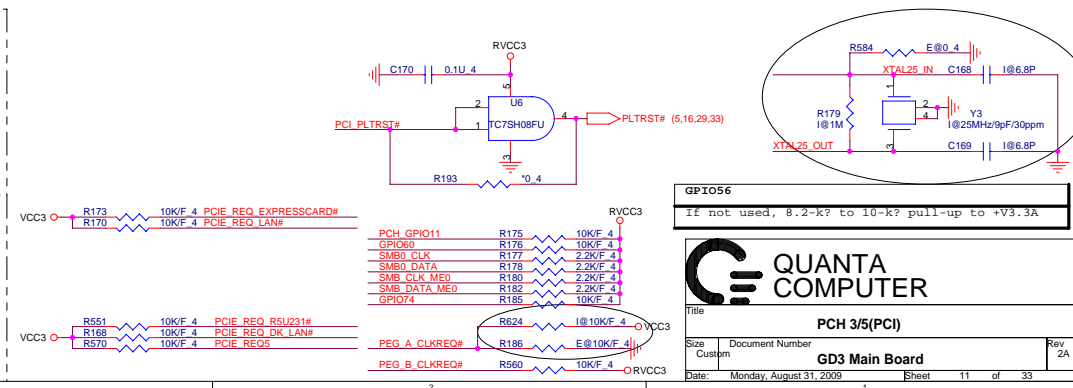
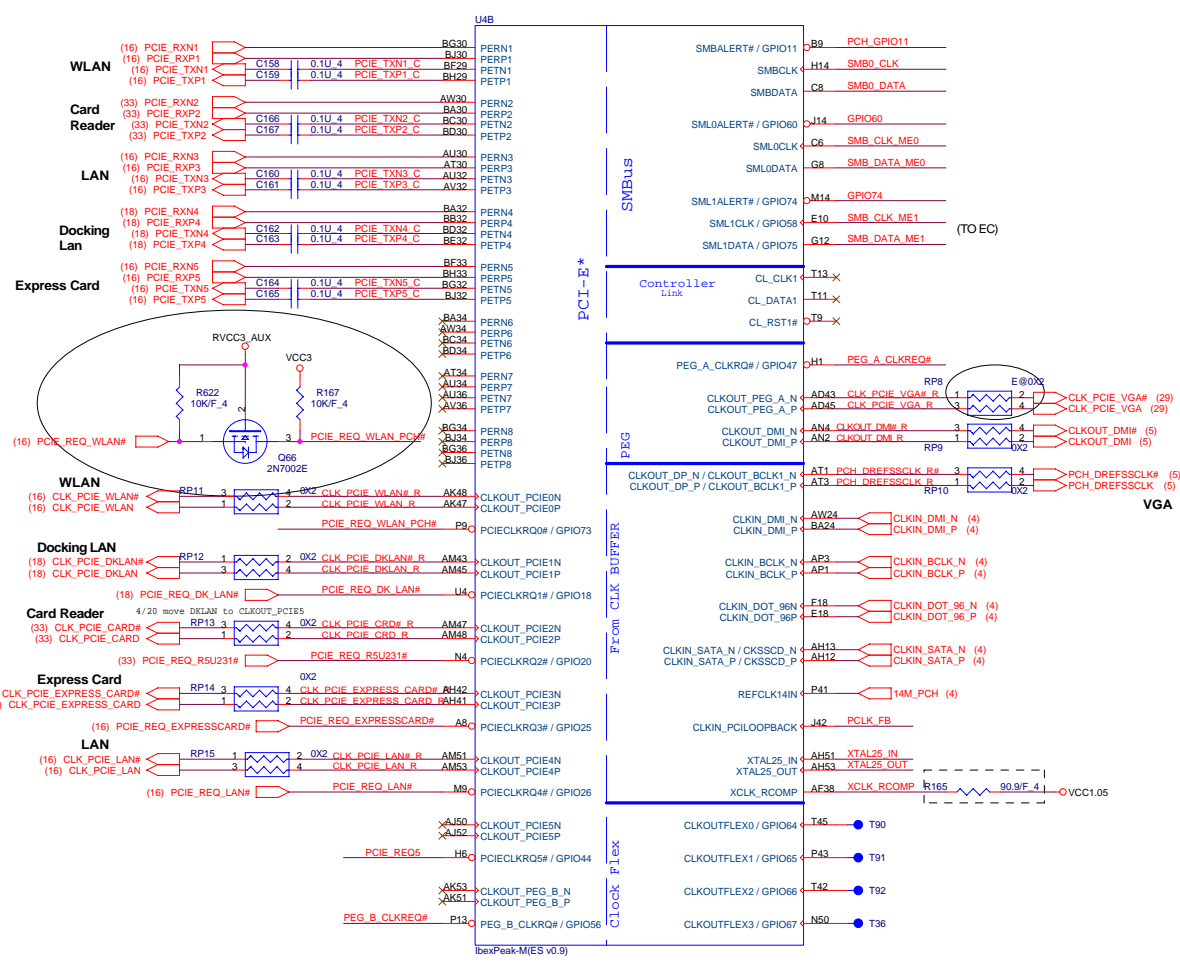




IBEX PEAK-M (PCI,USB,NVRAM)

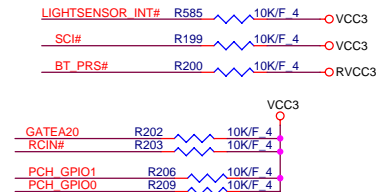
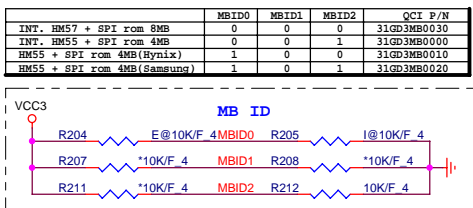
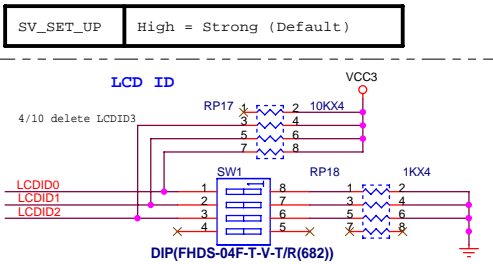
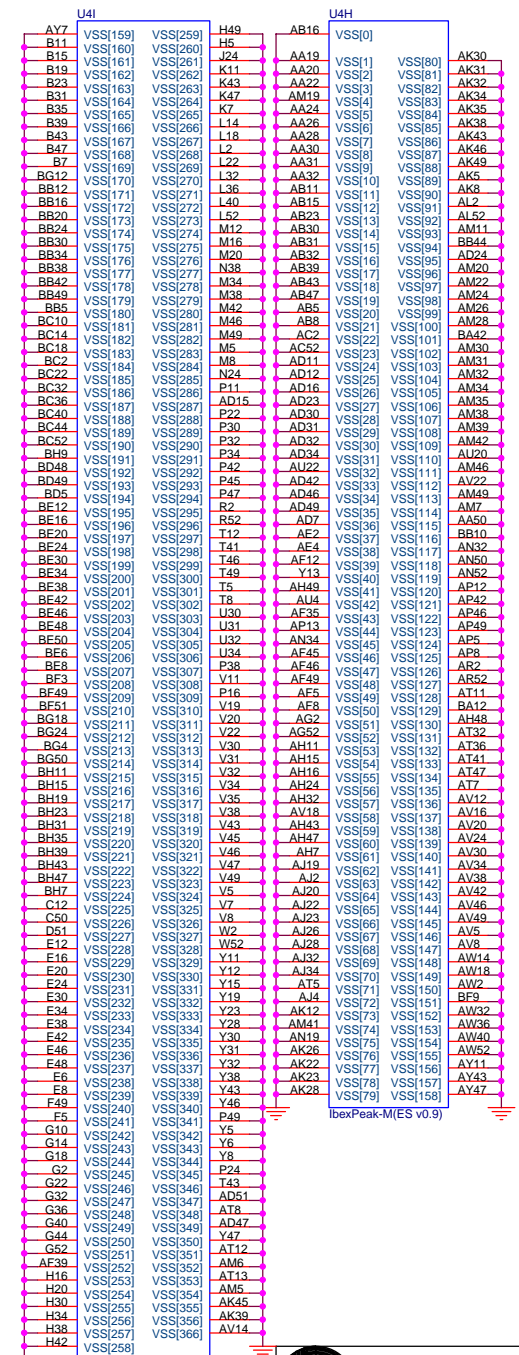
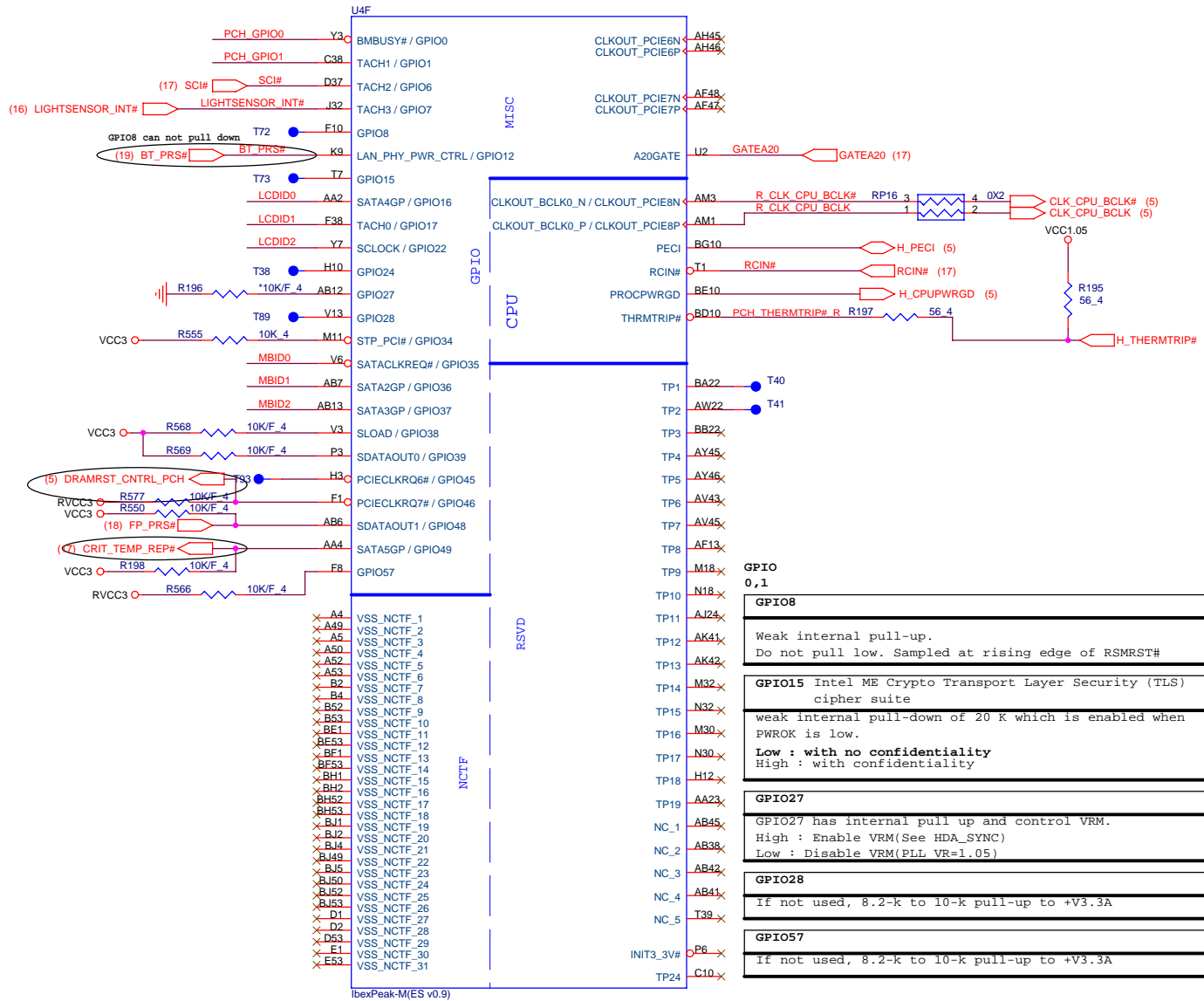


IBEX PEAK-M (PCI-E, SMBUS, CLK)



IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

12



1. Level 1 Environment-related Substances Should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

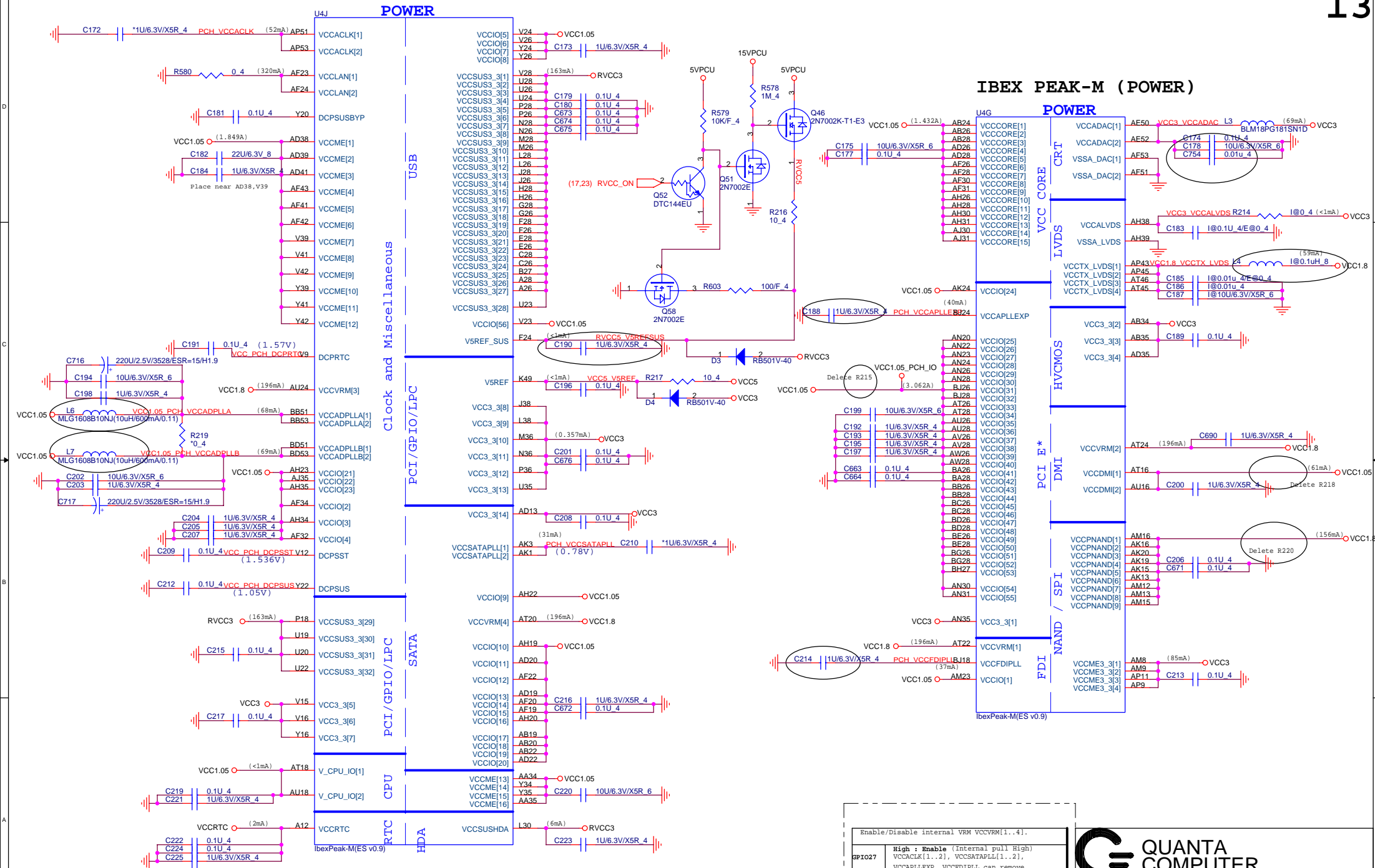
QUANTA COMPUTER

Title: **PCH 4/5(GPIO)**

Size: Custom Document Number: **GD3 Main Board** Rev: 1A

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IBEX PEAK-M (POWER)



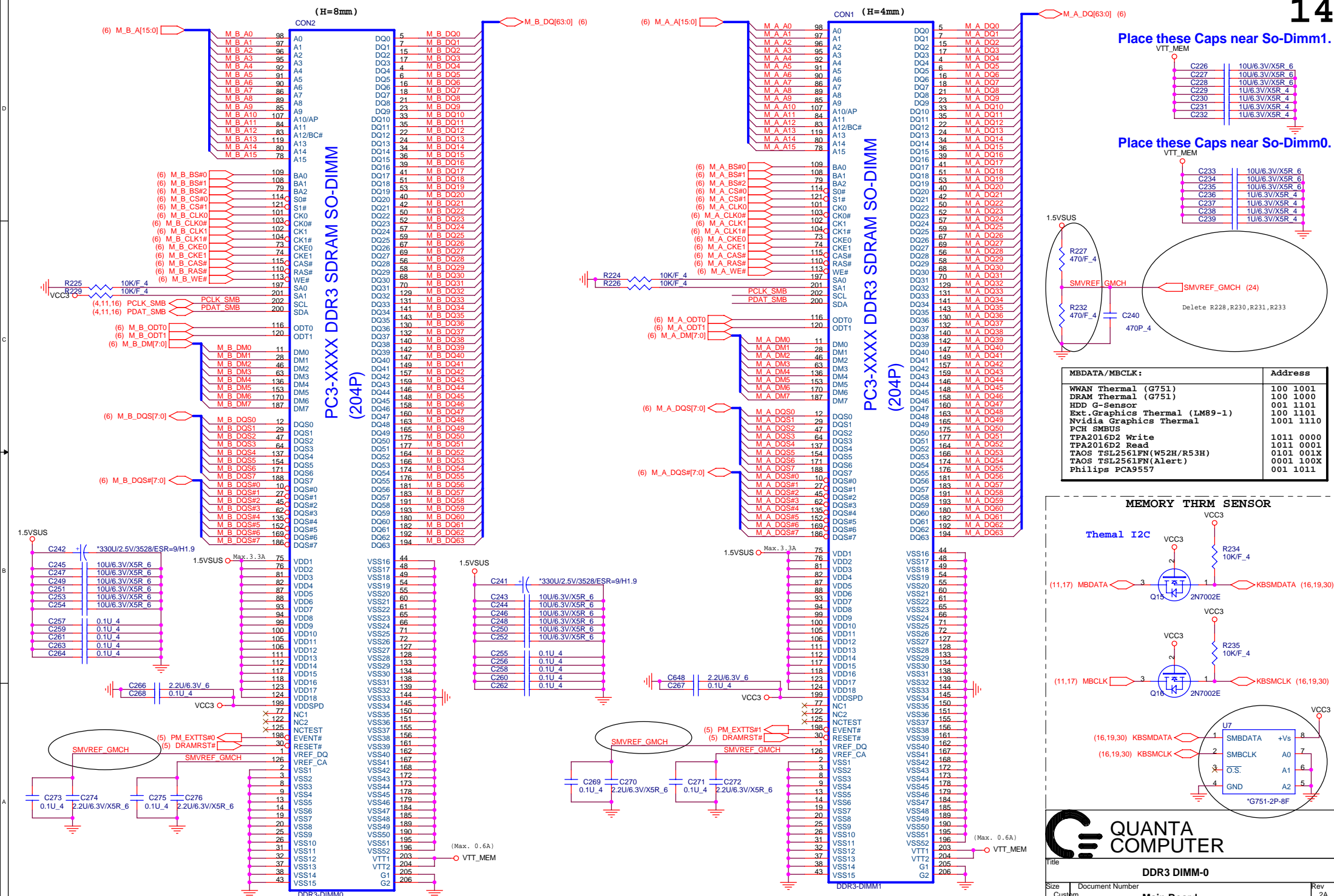
Enable/Disable internal VRM VCCVRM[1..4].	
GPIO27	High : Enable (Internal pull High) VCCVCL[1..2], VCCSATAPLL[1..2], VCCAPLLEXP, VCCFIDPLL can remove
	Low : Disable
Strapping VCC1.5 or VCC1.8	
HDA_SYNC	High : VCC1.5 Low : VCC1.8 (Internal pull Low)



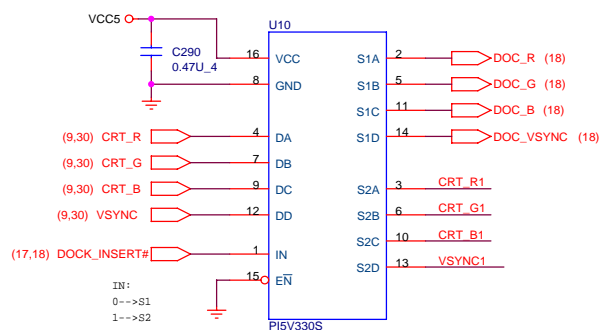
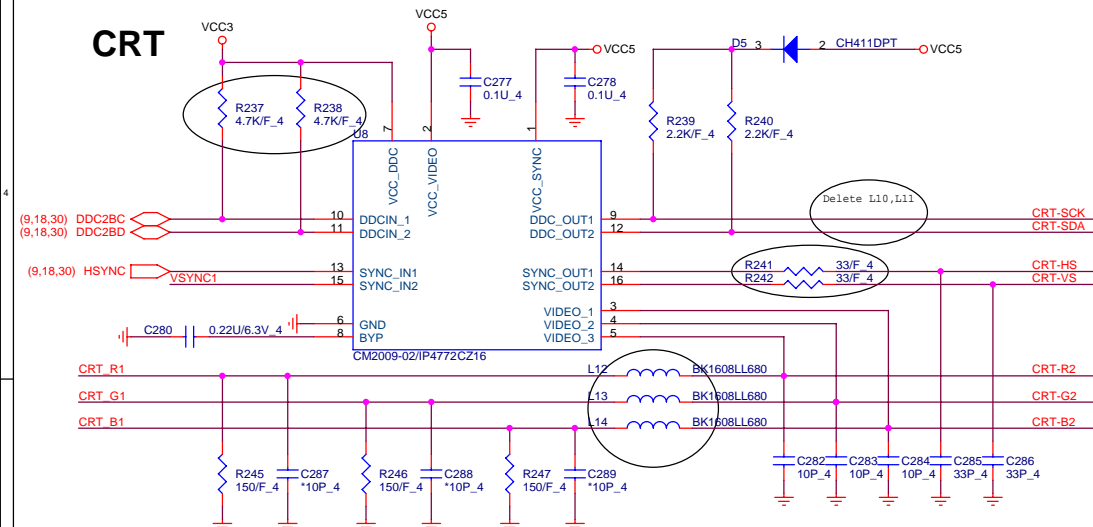
PCH 5/5(POWER)

GD3 Main Board

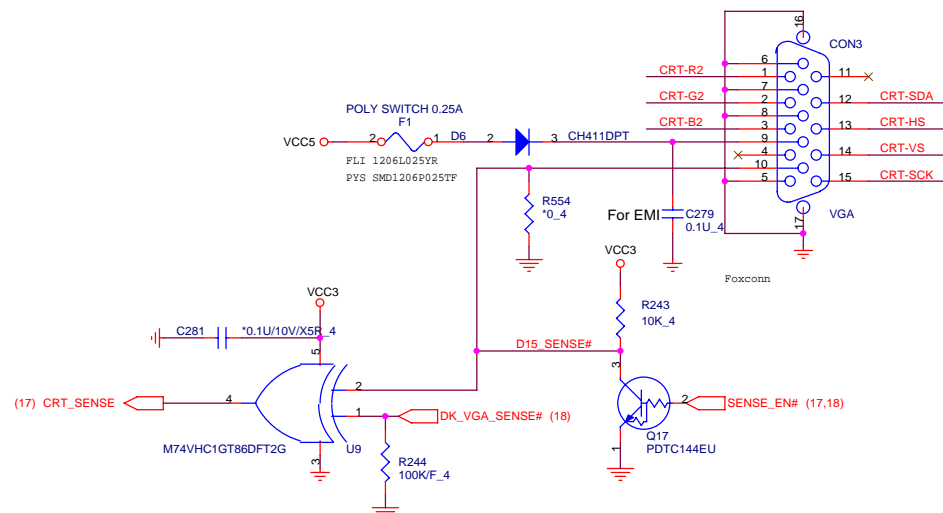
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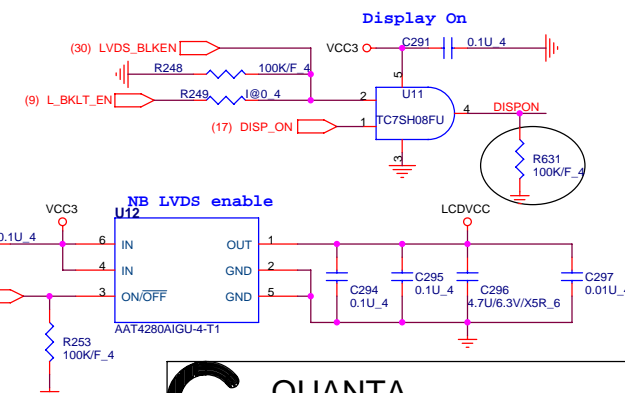
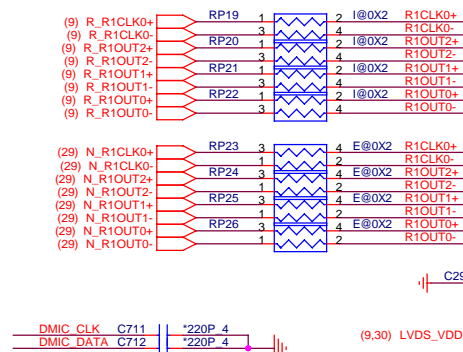
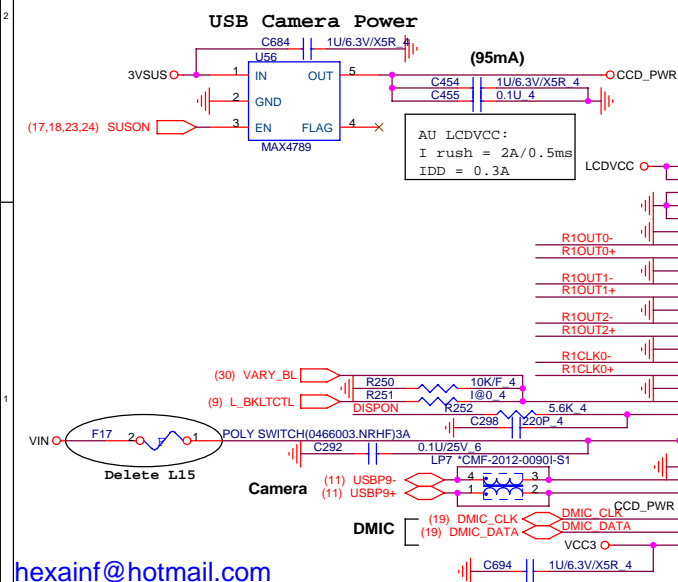
CRT



```
[EC Behavior]
CRT_SENSE: H=>L or L=>H detect which one is inserting
Docking_Insert#: H=>L detect which one is inserting
[CRT SW]
When Docking_Insert# is low switching RGB to Docking CRT
[SENSE_EN#]
Input for CRT pin10, EC assert to high when CRT
insert[NEO Request]
```



	SENSE_EN#	DK_VGA_SENSE#	D15_SENSE#	Docking_Insert#	CRT_SENSE#
Without Docking					
MB CRT no Plug	L	L	H	H	L
MB CRT Plug in	L	L	H => L	H	L => H
MB CRT plug out	L	L	L => H	H	H => L
With Docking					
All no Plug	L	L	H	L	L
MB CRT Plug in	L	L	H => L	L	L => H
MB CRT plug out	L	L	L => H	L	H => L
DOCK DVI Plug in	L	H => L	H	L	H => L
DOCK DVI Plug out	L	L => H	H	L	L => H
DOCK CRT Plug	L	H => L	H	L	H => L
DOCK CRT/DVI Plug	L	L => H	H	L	L => H



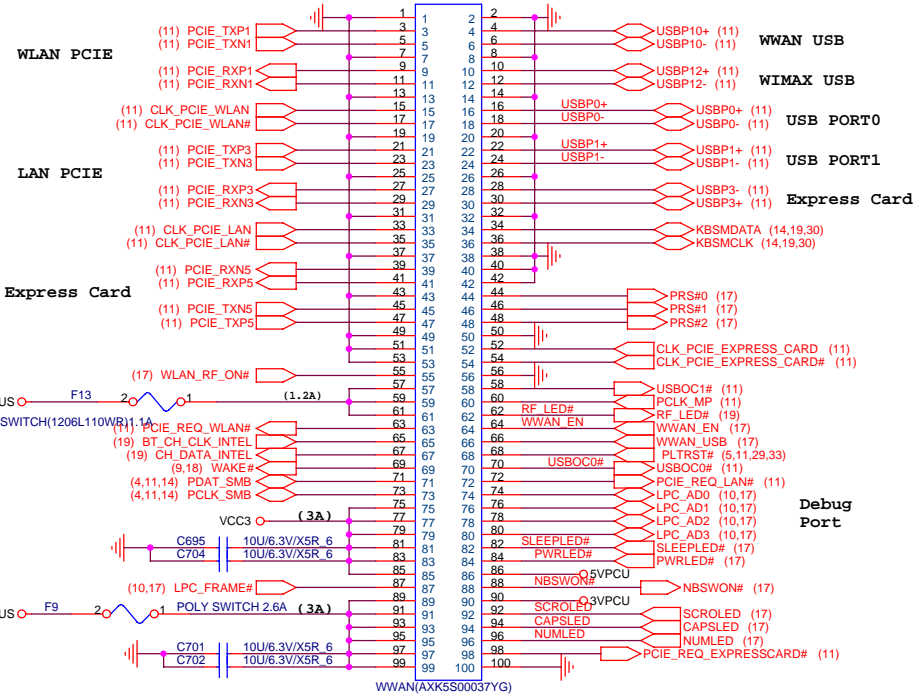
CRT/LVDS

Main Board

Rev	1A
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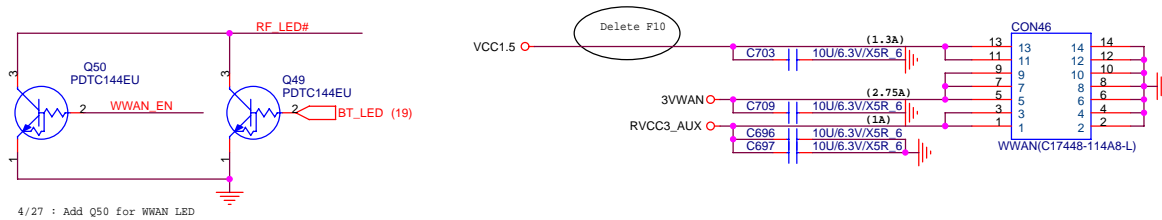
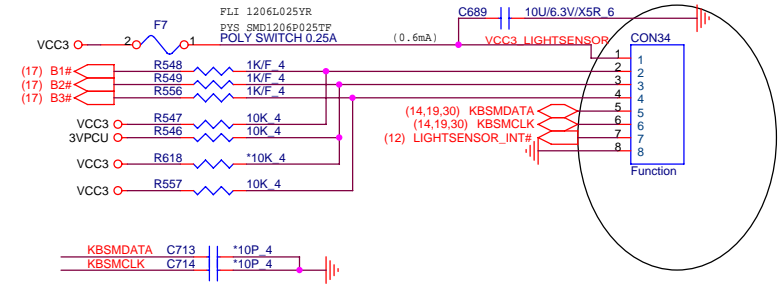
LAN Board BTB

CON38

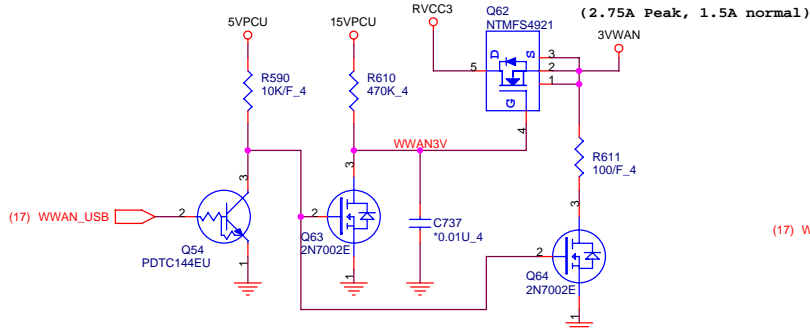


M/B to Function Board

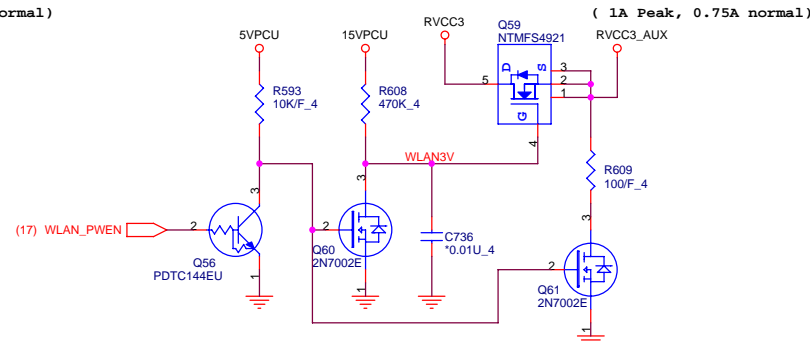
(FFC Type)



WWAN Power

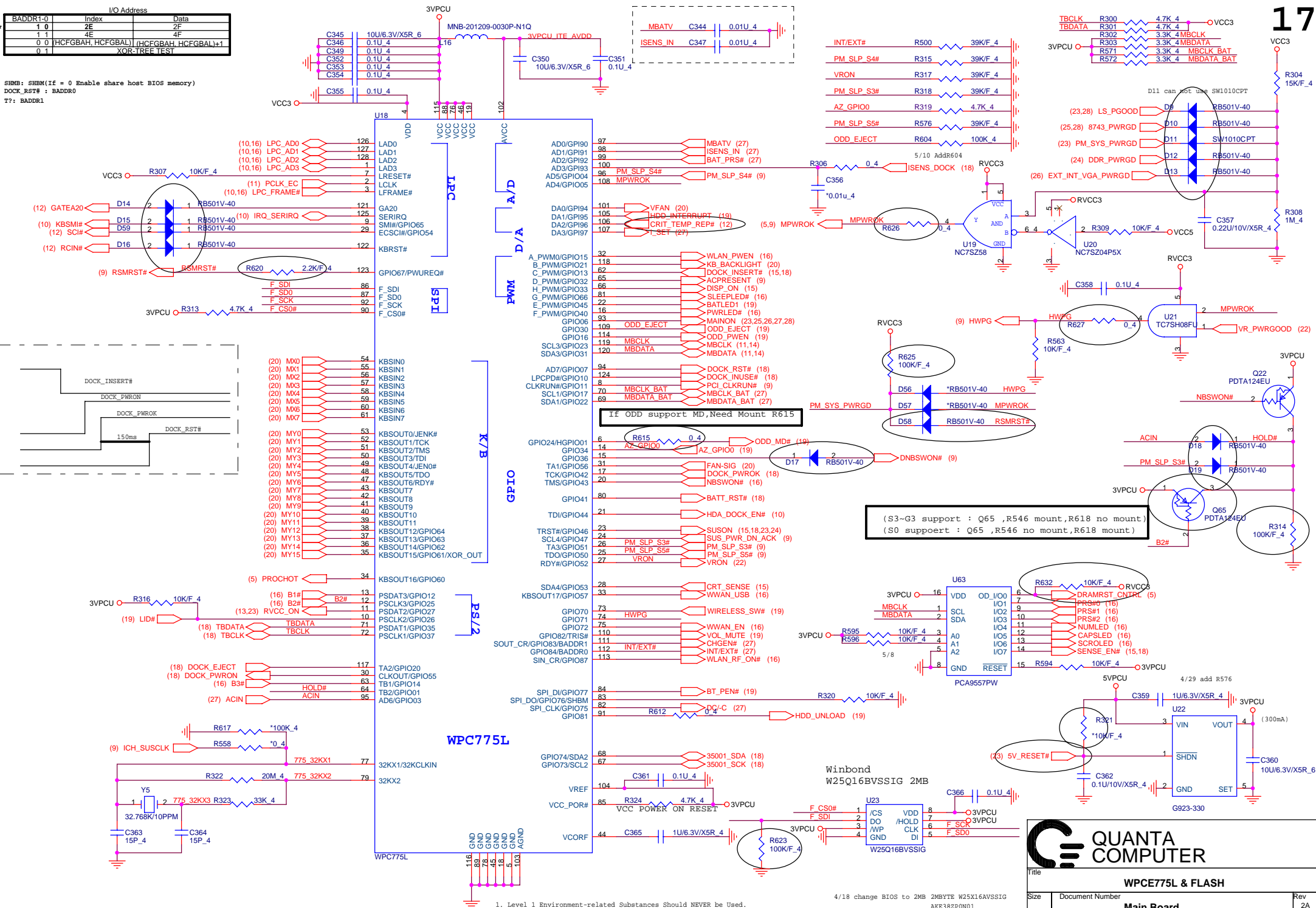


WLAN Power

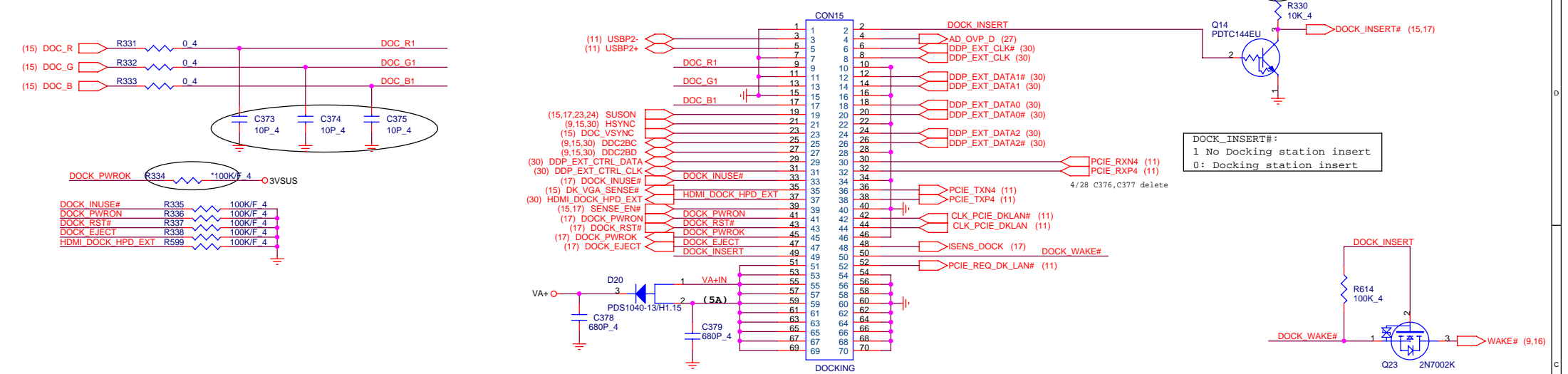


I/O Address		
BADDR1-0	Index	Data
1 0	2E	2F
1 1	4E	4F
0 0	(HCFGBAH, HCFGBAL) (HCFGBAH, HCFGBAL)+1	
0 1	XOR-TRF TEST	

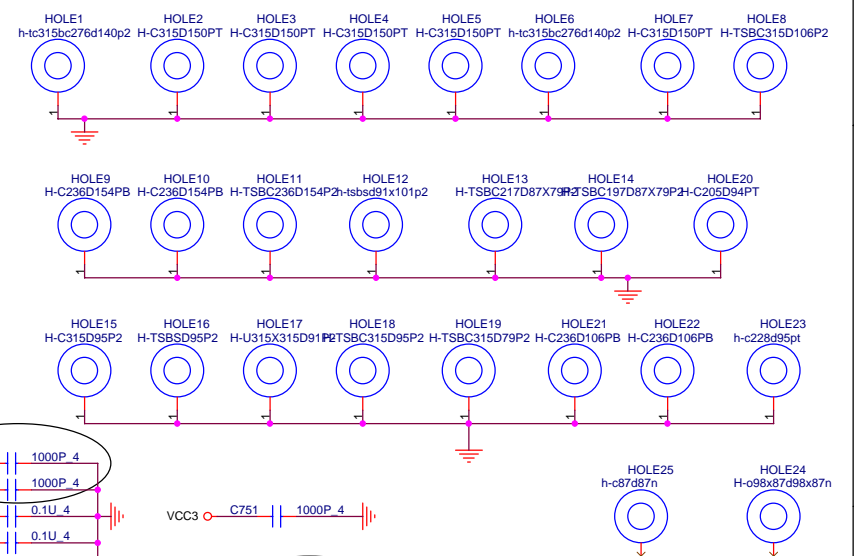
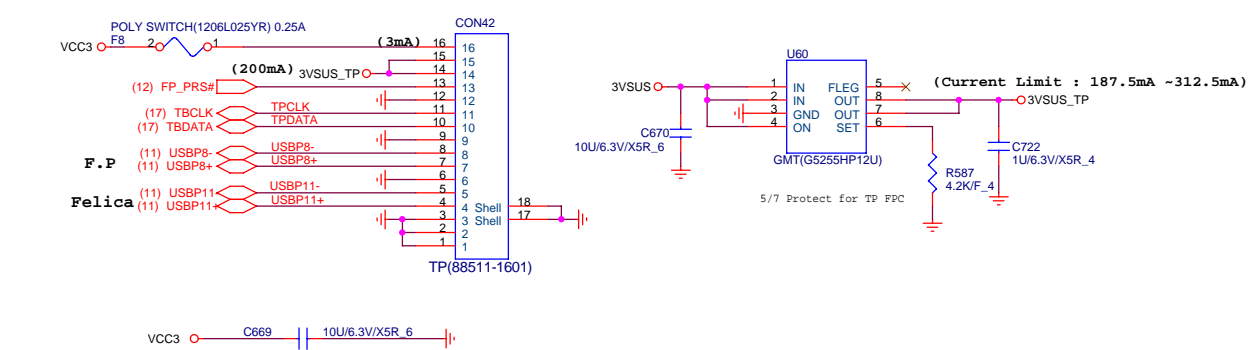
```
SHMB: SHBM(If = 0 Enable share host BIOS memory)
DOCK_RST# : BADDR0
T?: BADDR1
```



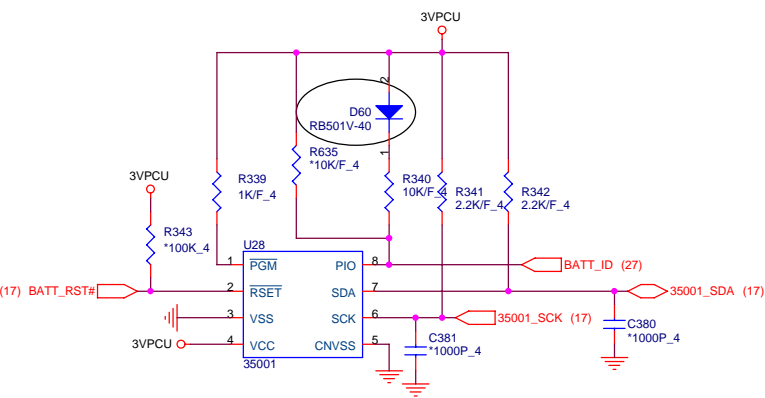
Docking



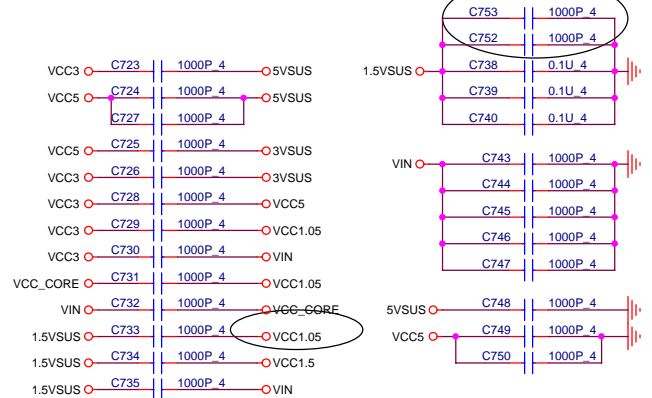
T/P to M/B (FPC)




35001



EMI



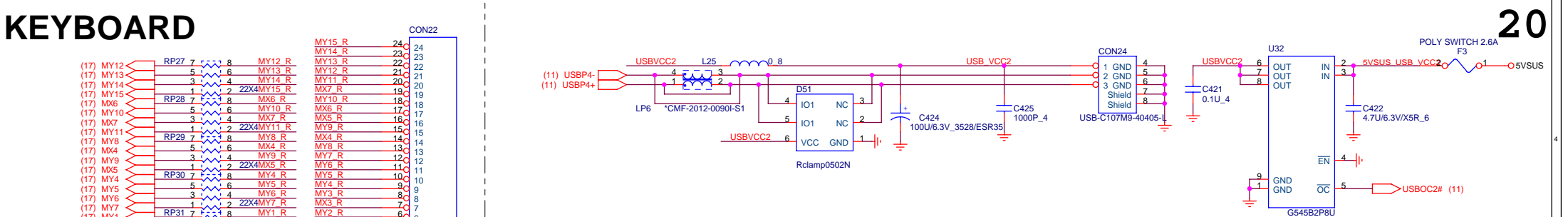


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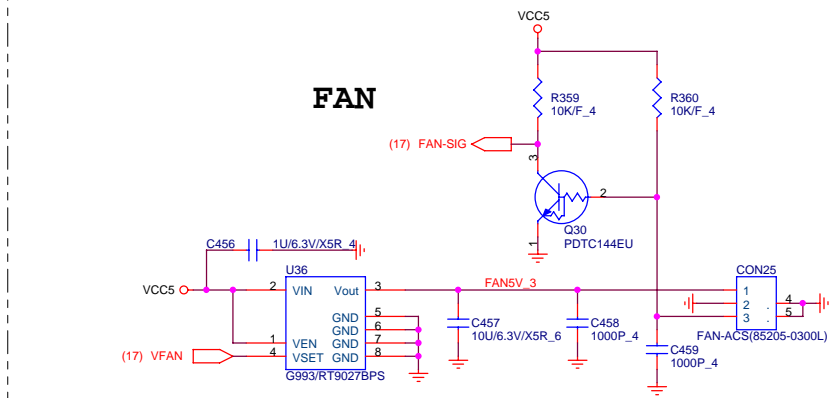
Title Docking/TPM/35001		
Size	Document Number	Rev 2A
Main Board		
Date:	Thursday, September 03, 2009	Sheet 18 of 33

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

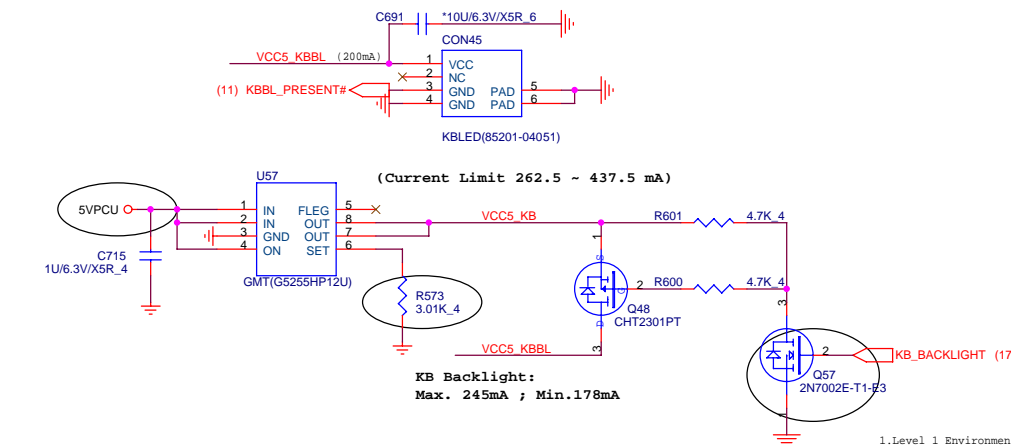
KEYBOARD




FAN



KB BACKLIGHT





QUANTA
COMPUTER

Title

KB/USB/FAN

Size

Document Number

Main Board

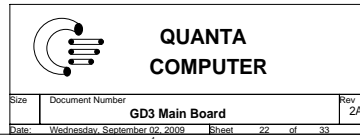
Rev 2A

Date: Monday, August 31, 2009

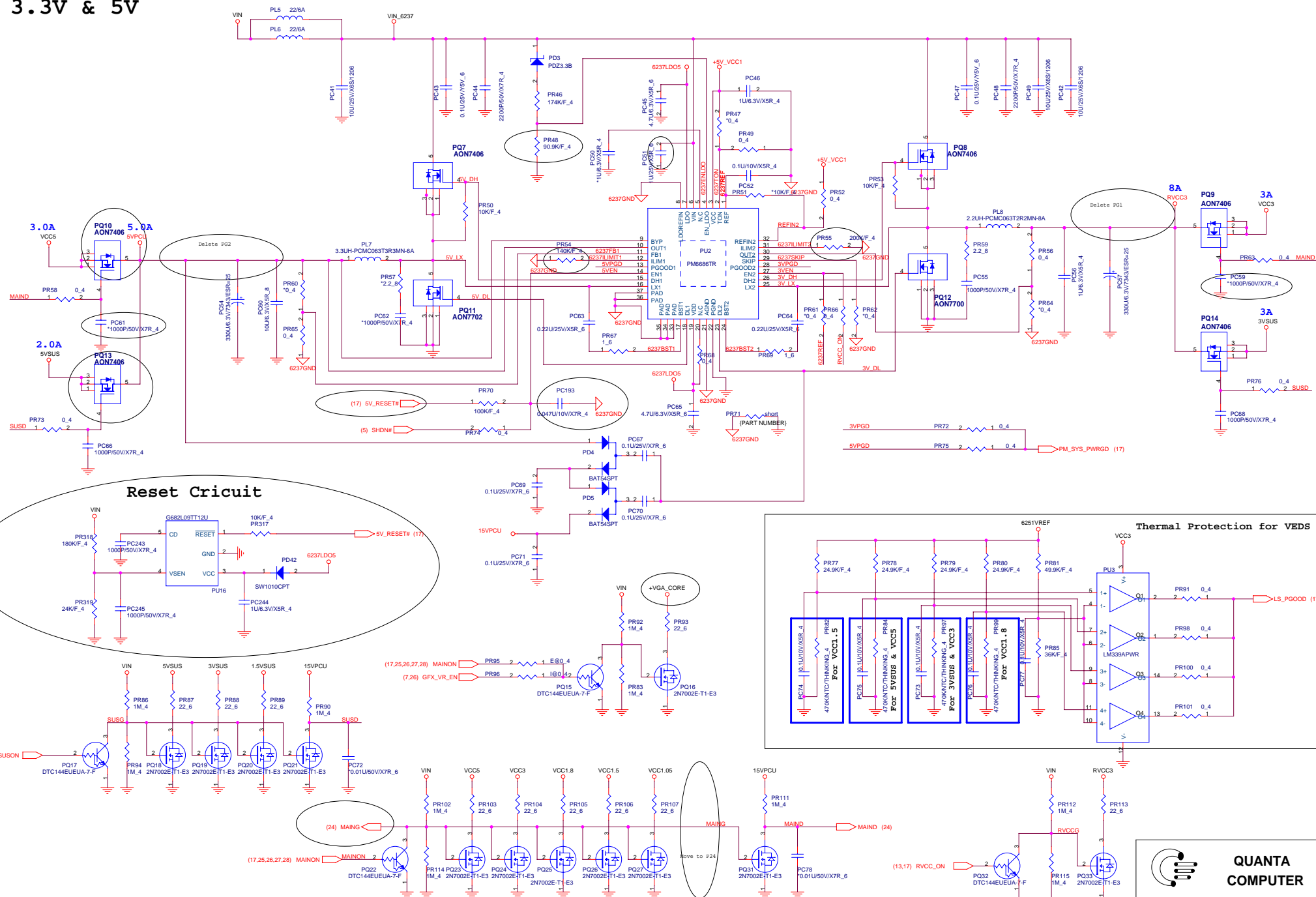
Sheet 20 of 33

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the Business Partners that Sony approves as Green Partners.

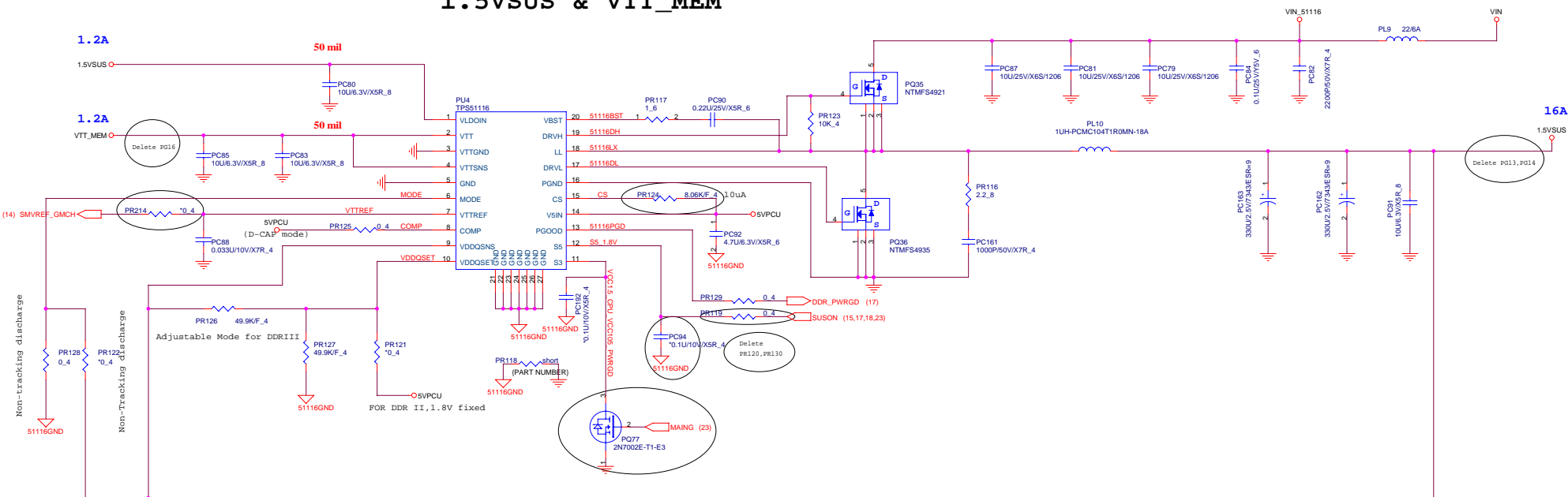




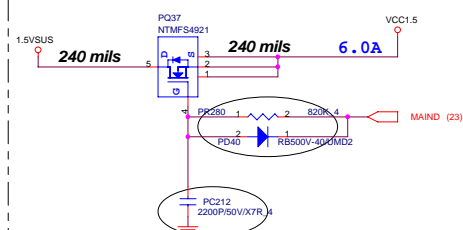
1. Level 1 Environment-related Substances Should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



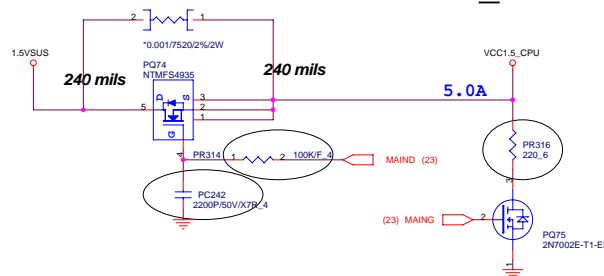
1.5VSUS & VTT_MEM



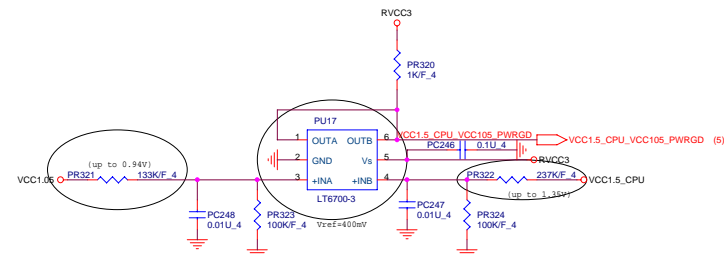
VCC1.5



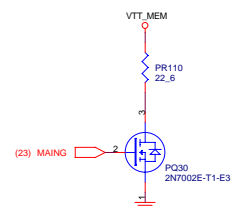
THE CIRCUIT NOT CHECK P/N **VCC1.5 CPU**
PR315



VCC1.5_CPU_VCC105_PWRGD



VTT_MEM Discharge

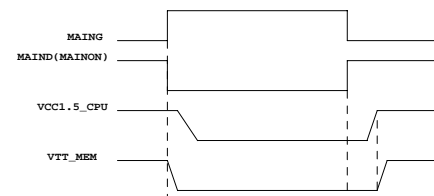


MODE	DISCHARGE MODE
+5V	No discharge
+1.8V	Tracking discharge
GND	Non-tracking discharge

VDDQSET	VDDQ(V)	VTTREF & VTT	NOTE
GND	2.5 fixed	VDDQSNS/2	DDR
5V	1.8 fixed	VDDQSNS/2	DDR2
FB-Resistor	Adjustable	VDDQSNS/2	1.5V<VDDQ<3V

$$V_{TT} = V_{TTREF} = V_{DDQSNS}/2 = 0.9V$$

STATE	S3	S5	1.8VSUS	VTTREF	VTI
S0	1	1	on	on	on
S3	0	1	on	on	off
S4/S5	0	0	off	off	off

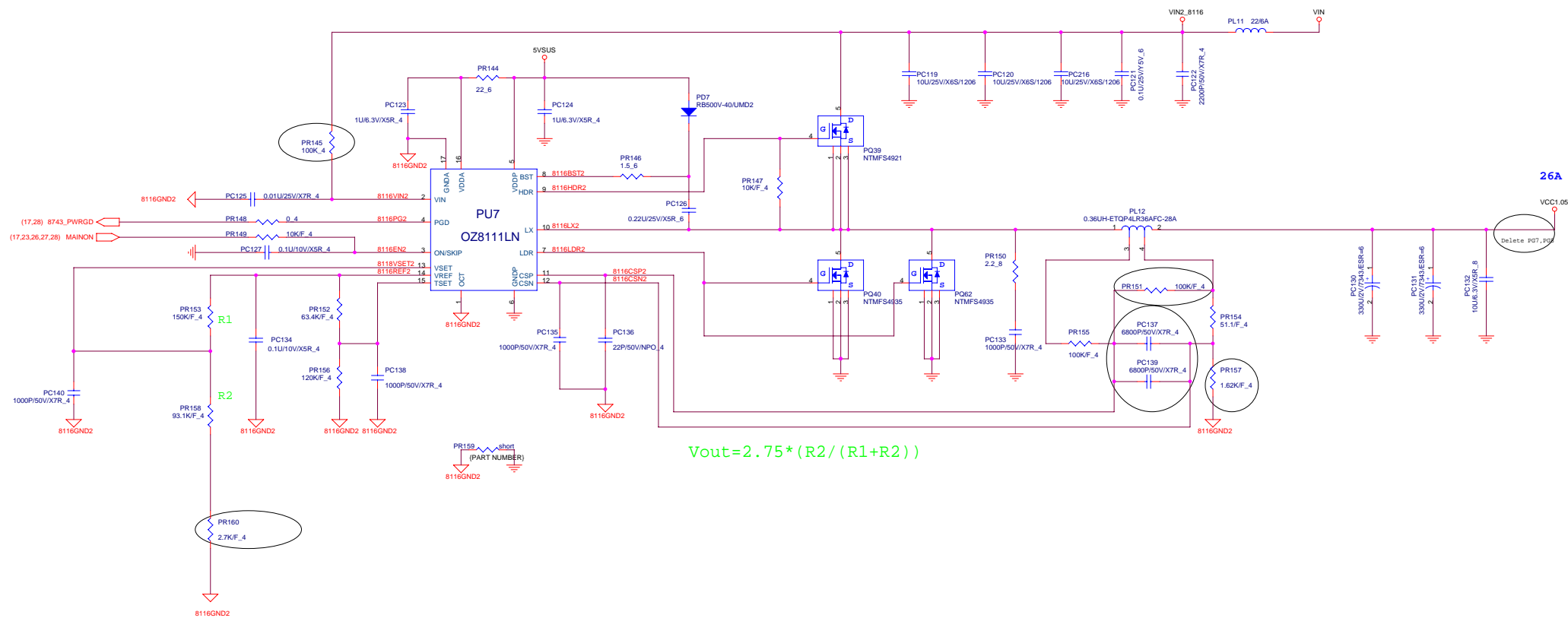


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	GD3 Main Board	2A
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1.Level 1 Environment-related Substances Should NEVER be Used

2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



(Ext. Graphice Plaes NDI
PQ41,PR161)

VTT_SEL	VCC1.05-1
High	1.05V
Low	1.10V

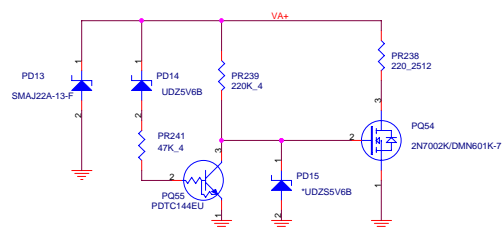
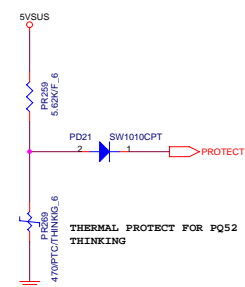


**QUANTA
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Size	Document Number	Rev
	GD3 Main Board	1A

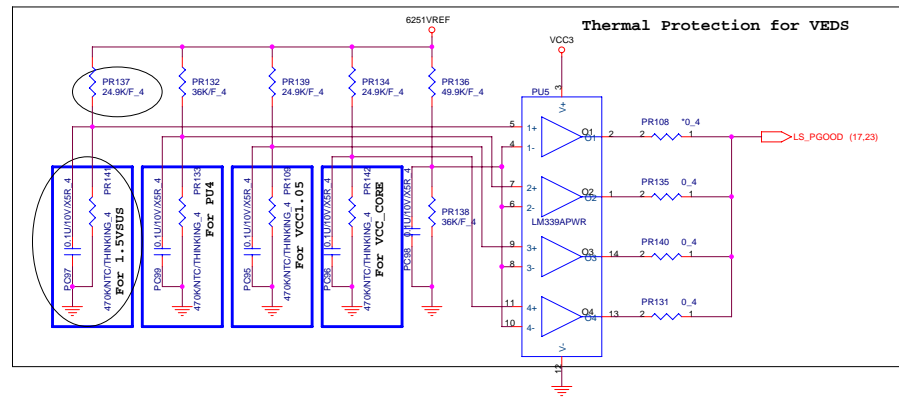
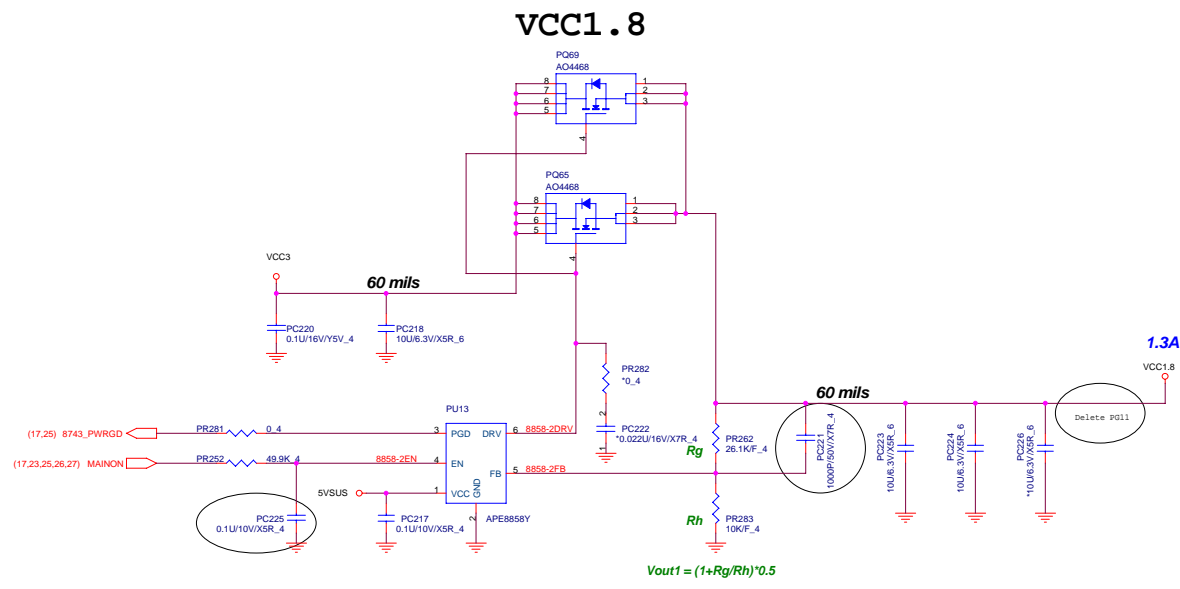
1.Level 1 Environment-related Substances Should NEVER be Used.

2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners. Date: Friday, September 04, 2009 Sheet 25 of 33



QUANTA
COMPUTER

Size	Document Number	Rev
	GD3 MB	1A
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nVidia VGA_CORE voltage setting:

V_PWRCNTL1	V_PWRCNTL0	VGA_VID	VGA_CORE
0	0	0101000	1.0V
0	1	0110100	0.85V
1	0	0111000	0.8V

Logical Strap Bit Mapping

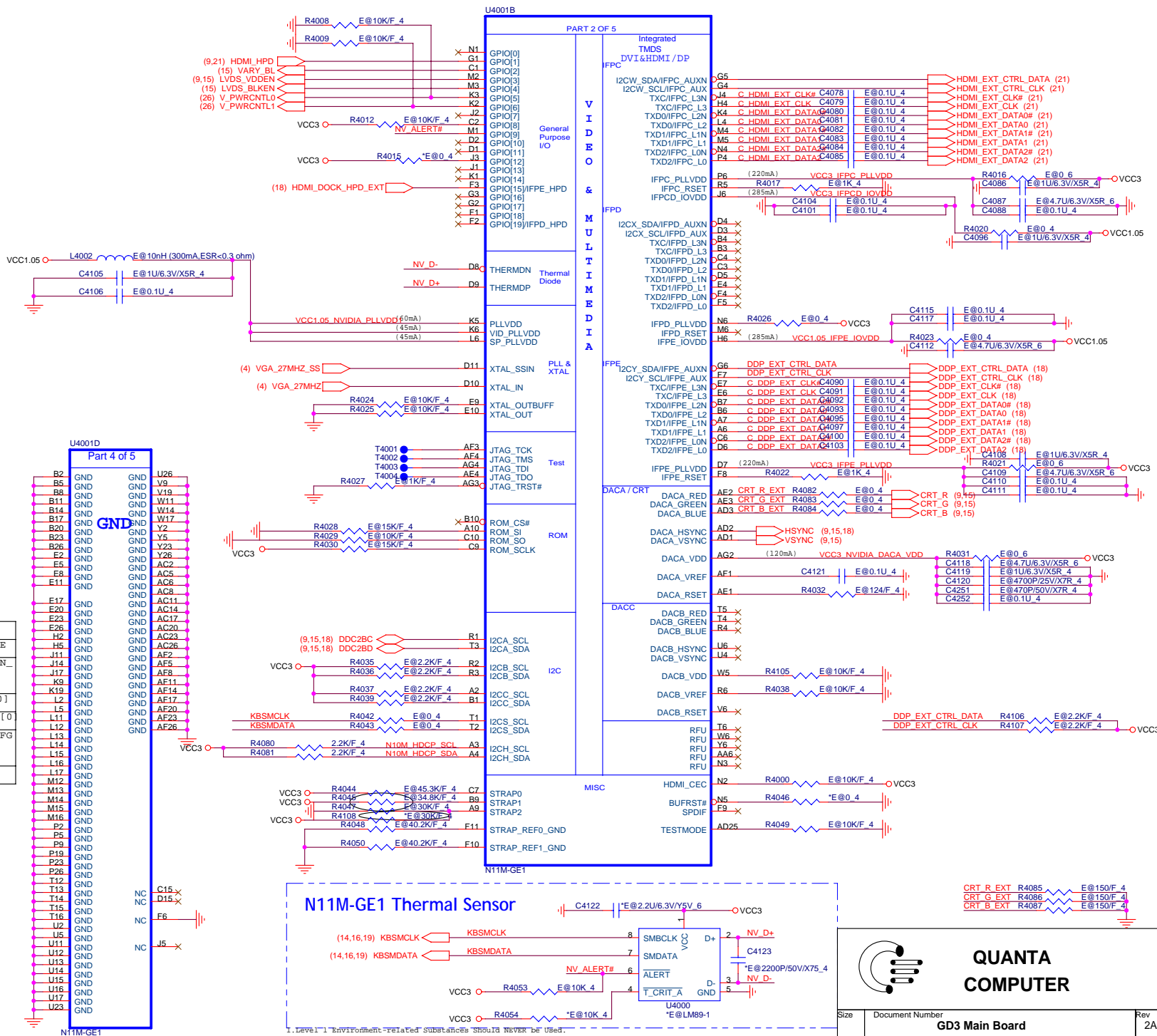
Resistor Value	Pull to VDD	Pull to GND
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Strap Bit Define

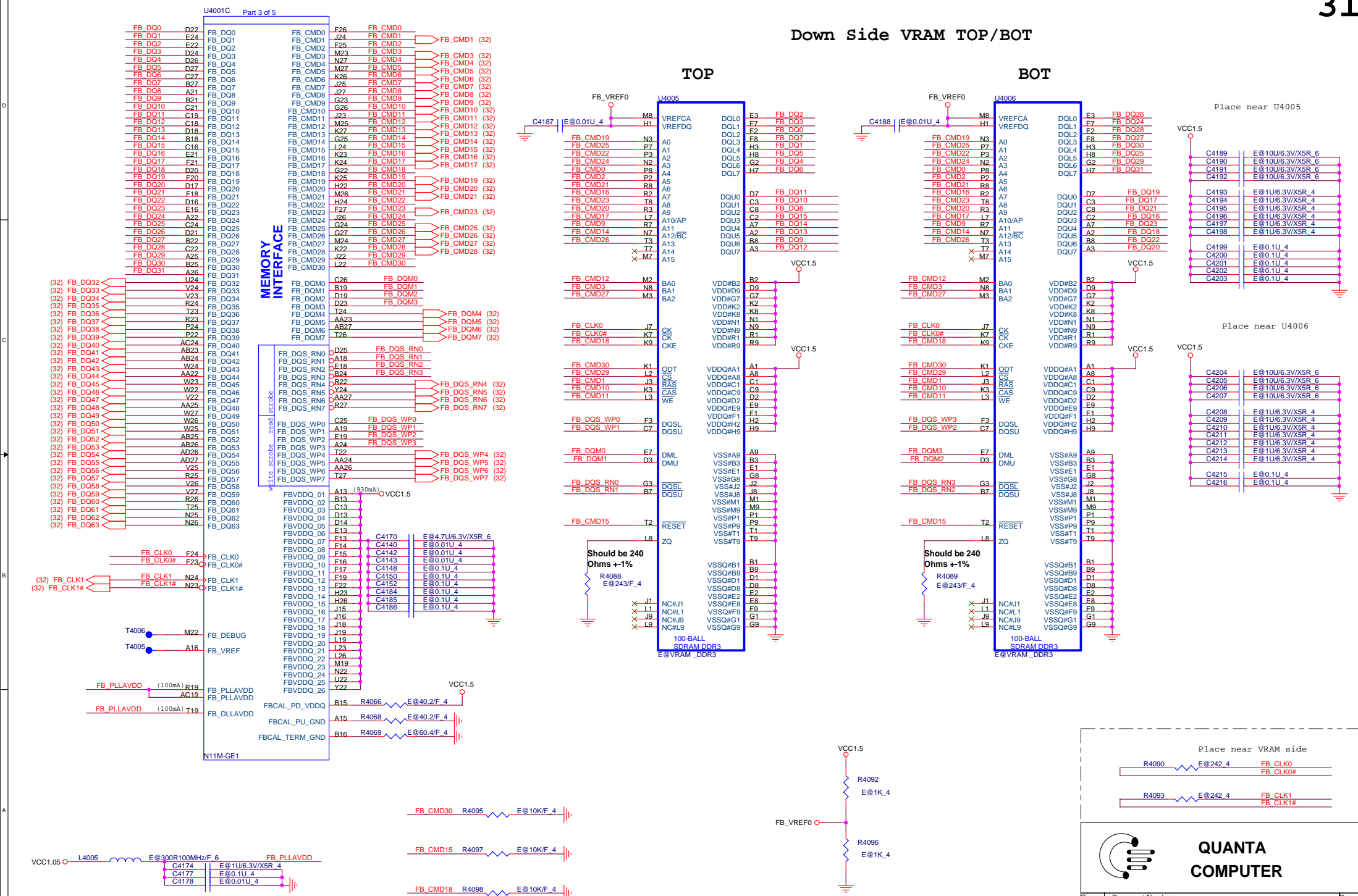
Straps	Bit 3	Bit 2	Bit 1	Bit 0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PL_LN_EN
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	3GIO_PADCFG	3GIO_PADCFG	3GIO_PADCFG	3GIO_PADCFG
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]

VRAM Strap:ROM_SI ; RAMCFG[x]

VRAM Capacity	VRAM Vender	ID	R4028
DDR3 64Mx16	Samsung	0011	PD20K
	Hynix	0010	PD15K



Down Side VRAM TOP/BOT



Up Side VRAM TOP/BOT

TOP

BOT

